# AU6431

## USB2.0 SD/MMC Single LUN Card Reader Controller

## Technical Reference Manual

Rev. 1.00

Jan. 2010

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## USB2.0 SD/MMC Single LUN Card
## Reader Controller

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# Revision History

| Date | Revision | Description |
|---|---|---|
| Sep 2009 | 0.10 | Preliminary Release |
| Sep 2009 | 0.20 | Fix the typo in pin assignment diagram |
| Jan 2010 | 1.00 | Official Release |

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# 1. Introduction
## 1.1 Description

The AU6431 is designed to deliver outstanding performance for data transmission between USB and compatible flash card interface. It supports USB 2.0 high-speed transferring to SD/MMC card. Besides, the AU6431 supports several operating systems, including MS Windows, LINUX and Mac OS.

The AU6431 integrates a high performance 8051 CPU as well as a splendidly efficient DMA hardware engine and internal 5V to 3.3V/3.3V to 1.8V regulators. The AU6431 provides manufacturers not merely BOM cost saving with the minimal numbers of components needed on the PCB but also smaller circuit board with the 24-pin QFN (4×4 mm) package.

In addition to high-speed 8051 CPU embedded and DMA hardware engine integrated, the AU6431 is fully compliant with USB Device Class Definition for Mass Storage and Bulk-Transport V1.0.Combination with these features, the AU6431 provides a completely ultra high performance USB2.0 card reader solution in a single chip.

AU6431 maximizes performance with the latest SD card specification available from the industry. Based on the features of low pin count and high performance characteristic, AU6431 supports a wide range of flash card reader applications used to digital camera, MP3 players, cell phone, PDA, camcorder, GPS device and so on to store many types of data, such as digital map, digital photos and compressed music.

## 1.2 Features

■General
- Fully compatible with USB2.0 High Speed and backward compatible with USB1.1 specifications
- Supports single LUN
- Supports both Windows and Mac OS
  - -Default Mass Storage Class driver comes from Windows ME/2000/XP/Vista/Windows 7 and Mac OS
  - -Windows 98 is supported by vendor driver from Alcor
- 24-pin QFN lead-free/Halogen-free/RoHS compliant package is available.

■Compliance
- Complies with USB Device Class Definition for Mass Storage and Bulk-Transport V1.0
- Complies with Secure Digital Card (SD) specification up to ver. 3.0(SDXC)
- Complies with MultiMedia Card (MMC) specification up to ver. 4.3, 4-bit data bus.

■Benefit
- 1K bytes of ping-pong FIFO buffs the data transmission between transmitter and receiver
- Integrated hardware DMA engine enhances overall performance of data transfers
- User-friendly Dynamic icon utility software can display icon message upon insertion/removal of compatible flash cards under Windows
- Optimizes performance via multiple sectors transfer
- Built-in 5V to 3.3V and 3.3V to 1.8V regulator offers customers lower BOM cost

# 2. Application Block Diagram

Following application diagram demonstrates a typical card reader using the AU6431 chip. By connecting the card reader to a desktop or notebook PC through USB bus, the AU6431 becomes a bus-powered, high speed USB card reader, which can be used as a bridge for data transfer between Desktop PC and Notebook PC.

**Figure 2.1 Block Diagram**
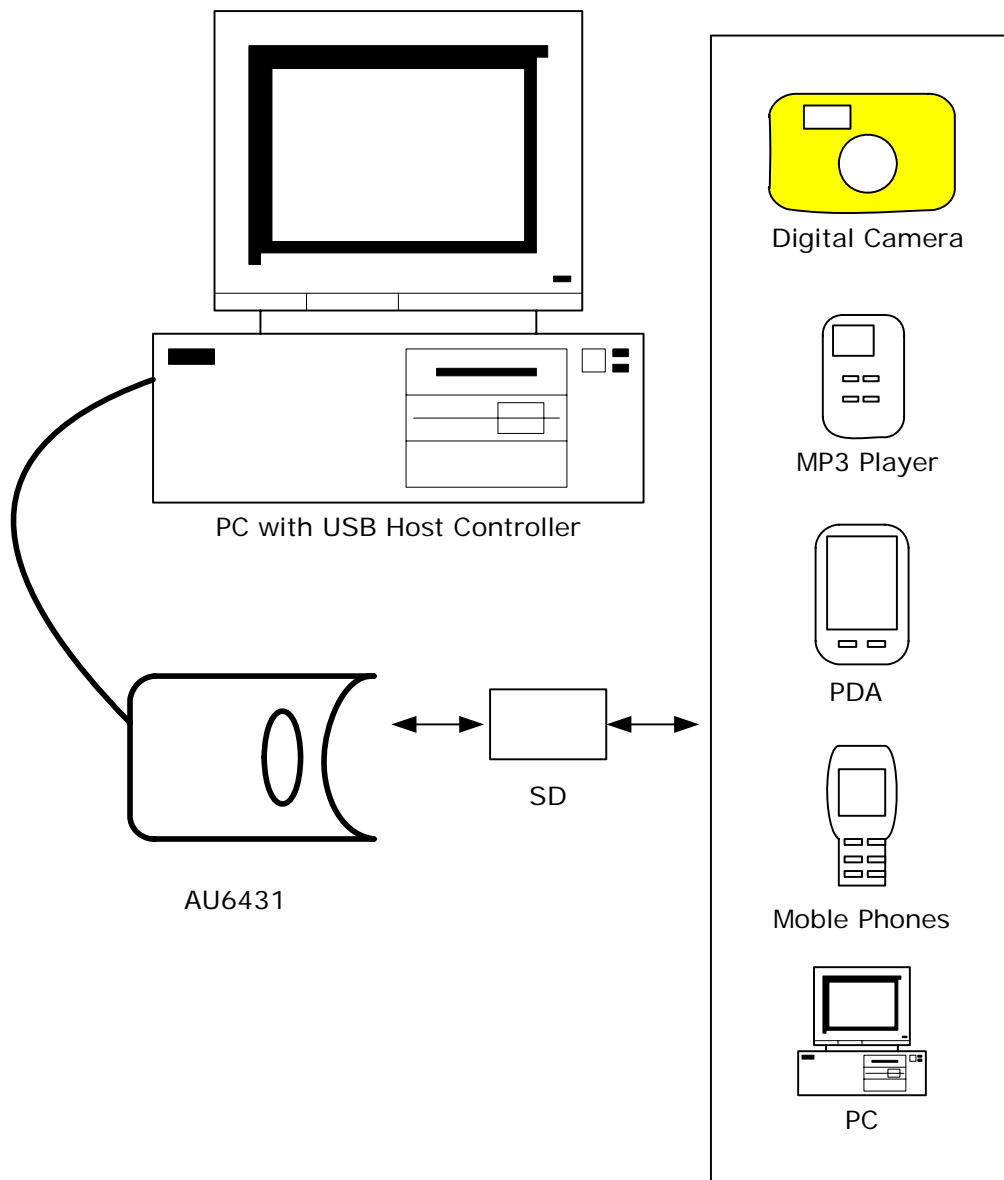
# 3. Pin Assignment

AU6431 is available in 24-pin QFN package.   Below diagram shows signal name of each pin and table in the following page describes each pin in detail.

**Figure 3.1 AU6431 Pin Assignment Diagram**

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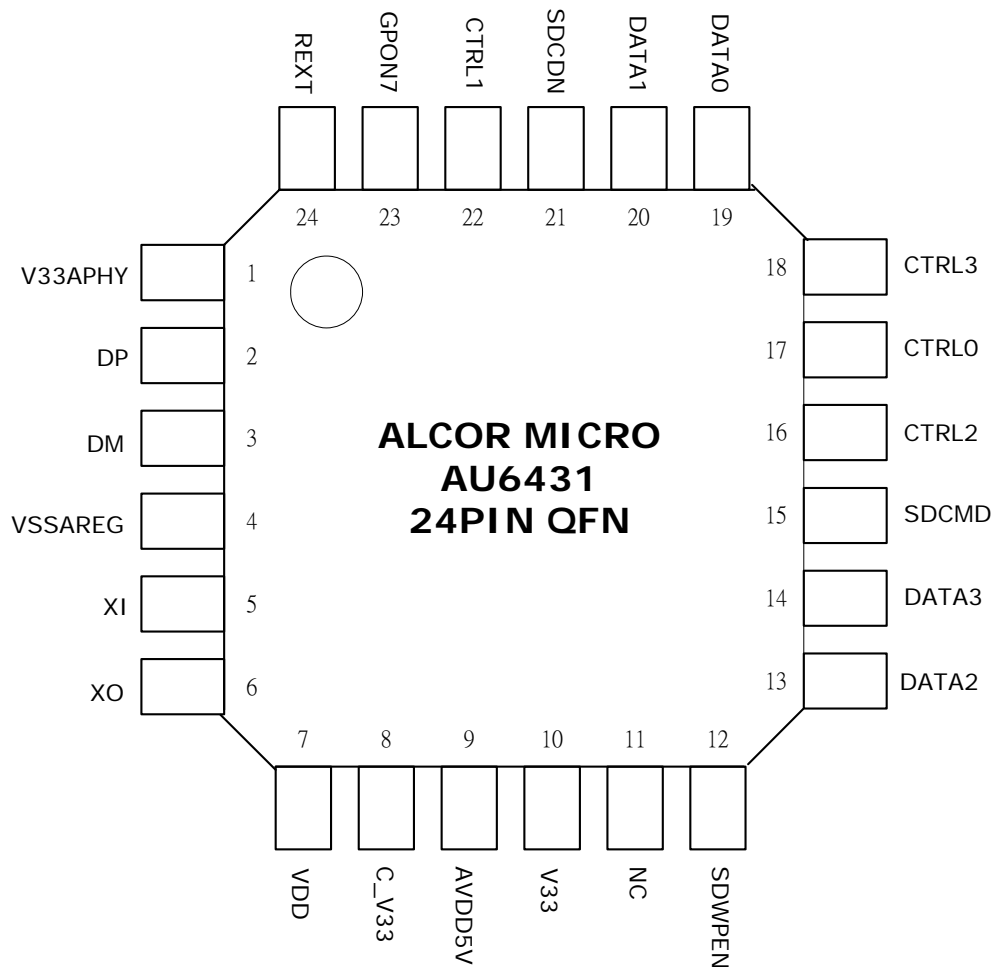
## Table 3.1 AU6431 Pin Descriptions

| Pin # | Pin Name | I/O | Description |
|-------|----------|-----|-------------|
| 1 | V33APHY | | PHY 3.3V power pin |
| 2 | DP | | USB DP |
| 3 | DM | | USB DM |
| 4 | VSSAREG | | PHY Ground pin |
| 5 | XI | I | Crystal input |
| 6 | XO | O | Crystal output |
| 7 | VDD | | Core 1.8V power |
| 8 | C_V33 | | Card power 3.3V output |
| 9 | AVDD5V | | Regulator 5V input |
| 10 | V33 | | Regulator 3.3V output |
| 11 | NC | | |
| 12 | SDWPEN | I | SDWPEN<br>'1' for depends on SDWP [default]<br>'0' for SDWP disable (SD always writable) |
| 13 | DATA2 | IO | SDDATA2 |
| 14 | DATA3 | IO | SDDATA3 |
| 15 | SDCMD | IO | SDCMD |
| 16 | CTRL2 | IO | EEPCLK |
| 17 | CTRL0 | IO | SDCLK |
| 18 | CTRL3 | IO | EEPDAT |
| 19 | DATA0 | IO | SDDATA0 |
| 20 | DATA1 | IO | SDDATA1 |
| 21 | SDCDN | IO | SDCDN |
| 22 | CTRL1 | IO | SDWP |
| 23 | GPON7 | O | Card access LED. |
| 24 | REXT | | 680 Ω reference resistance |
| DiePad | GND | GND | Ground |

# 4. System Architecture and Reference Design

## 4.1 AU6431 Block Diagram

**Figure 4.1 AU6431 Block Diagram**
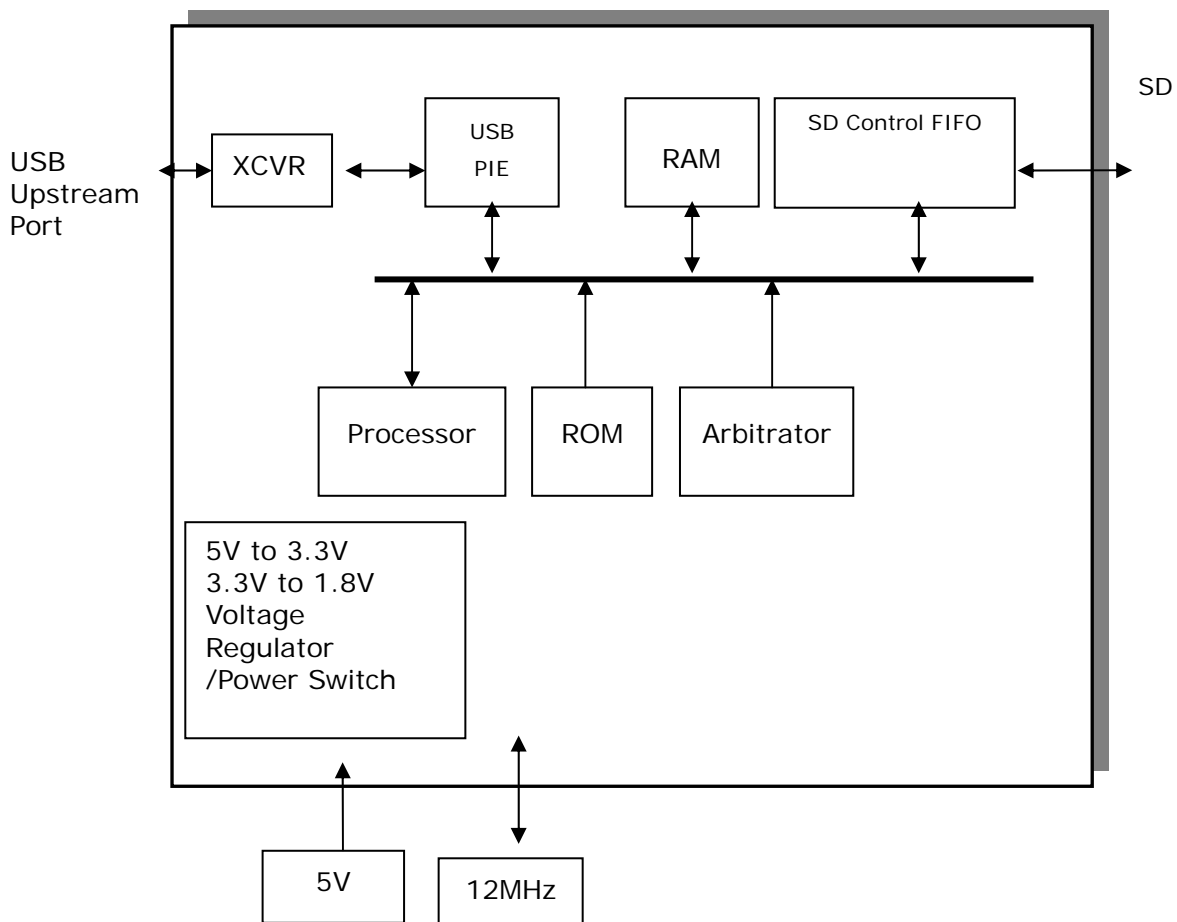
# 5. Electrical Characteristics

## 5.1 Absolute Maximum Ratings

### Table 5.1 Absolute Maximum Ratings

| SYMBOL | PARAMETER | RATING | UNITS |
|--------|-----------|--------|-------|
| AVDD5V | Power supply | -1 to 4V | V |
| $V_{IN}$ | Input Signal Voltage | -1 to 4V | V |
| $T_{STG}$ | Storage Temperature | -40 to 150 | $^{O}C$ |

## 5.2 Recommended Operating Conditions

### Table 5.2 Recommended Operating Conditions

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS |
|--------|-----------|-----|-----|-----|-------|
| AVDD5V | Power Supply | 4.75 | | 5.25 | V |
| $V_{IN}$ | Input Signal Voltage | -0.3 | | VCC33 +0.3 | V |
| $T_{OPR}$ | Operating Temperature | 0 | | 85 | $^{O}C$ |

## 5.3 General DC Characteristics

### Table 5.3 General DC Characteristics

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------|-----------|-----------|-----|-----|-----|-------|
| $I_{IN}$ | Input current | No pull-up or pull-down | -10 | $\pm1$ | 10 | $\mu A$ |
| $I_{OZ}$ | Tri-state leakage current | | -10 | $\pm1$ | 10 | $\mu A$ |
| $C_{IN}$ | Input capacitance | Pad Limit | | 2.8 | | $\rho F$ |
| $C_{OUT}$ | Output capacitance | Pad Limit | | 2.8 | | $\rho F$ |
| $C_{BID}$ | Bi-directional buffer capacitance | Pad Limit | | 2.8 | | $\rho F$ |
| $I_{CC}$ | Operating supply current | Without Memory Card | | | 0.2 | mA |

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## 5.4 DC Electrical Characteristics of 3.3V I/O Cells

### Table 5.4 DC Electrical Characteristics of 3.3V I/O Cells

| SYMBOL | PARAMETER | CONDITIONS | Limits | | | UNIT |
|--------|-----------|------------|--------|--------|--------|------|
| | | | MIN | TYP | MAX | |
| $V_{D33P}$ | Power supply | 3.3V I/O | 3.0 | 3.3 | 3.6 | V |
| $V_{il}$ | Input low voltage | LVTTL | | | 0.8 | V |
| $V_{ih}$ | Input high voltage | | 2.0 | | | V |
| $V_{ol}$ | Output low voltage | $|I_{ol}|$ =2~16mA | | | 0.4 | V |
| $V_{oh}$ | Output high voltage | $|I_{oh}|$ =2~16mA | 2.4 | | | V |
| $R_{pu}$ | Input pull-up resistance | PU=high, PD=low | 55 | 75 | 110 | K$\Omega$ |
| $R_{pd}$ | Input pull-down resistance | PU=low, PD=high | 40 | 75 | 150 | K$\Omega$ |
| $I_{in}$ | Input leakage current | $V_{in}= V_{D33P}$ or 0 | -10 | $\pm$1 | 10 | $\mu$A |
| $I_{oz}$ | Tri-state output leakage current | | -10 | $\pm$1 | 10 | $\mu$A |

## 5.5 USB Transceiver Characteristics

### Table 5.5 Electrical characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--------|-----------|------------|------|------|------|------|
| V33AREG | Analog supply Voltage | | 3.0 | 3.3 | 3.6 | V |
| VDD | Digital supply Voltage | | 1.62 | 1.8 | 1.98 | V |

### Table 5.6 Static characteristic：Digital pin

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--------|-----------|------------|------|------|------|------|
| Input levels | | | | | | |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $V_{IH}$ | High-level input voltage | | 2.0 | | | V |
| Output levels | | | | | | |
| $V_{OL}$ | Low-level output voltage | | | | 0.2 | V |
| $V_{OH}$ | High-level output voltage | | VD33P-0.2 | | | V |

### Table 5.7 Static characteristic：Analog I/O pins（DP/DM）

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|--------|-----------|------------|------|------|------|------|
| USB2.0 Transceiver（HS） | | | | | | |
| Input Levels（differential receiver） | | | | | | |
| $V_{HSDIFF}$ | High speed differential input sensitivity | ｜$V_{I（DP）}$-$V_{I（DM）}$｜ measured at the connection as application circuit | 300 | | | mV |
| $V_{HSCM}$ | High speed data signaling common mode voltage range | | -50 | | 500 | mV |
| $V_{HSSQ}$ | High speed squelch detection threshold | Squelch detected | | | 100 | mV |
| | | No squelch detected | 150 | | | mV |
| $V_{HSDSC}$ | High speed disconnection detection threshold | Disconnection detected | 625 | | | mV |
| | | Disconnection not detected | | | 525 | mV |
| Output Levels | | | | | | |
| $V_{HSOI}$ | High speed idle level output voltage(differential) | | -10 | | 10 | mV |
| $V_{HSOL}$ | High speed low level output voltage(differential) | | -10 | | 10 | mV |
| $V_{HSOH}$ | High speed high level output voltage(differential) | | 360 | | 440 | mV |
| $V_{CHIRPJ}$ | Chirp-J output voltage（differential） | | 700 | | 1100 | mV |
| $V_{CHIRPK}$ | Chirp-K output voltage（differential） | | -900 | | -500 | mV |
| Resistance | | | | | | |
| $R_{DRV}$ | Driver output impedance | Equivalent resistance used as internal chip only | 3 | 6 | 9 | Ω |

| | | Overall resistance including external resistor | 40.5 | 45 | 49.5 | |
|---|---|---|---|---|---|---|
| Termination | | | | | | |
| V<sub>TERM</sub> | Termination voltage for pull-up resistor on pin RPU | | 3.0 | | 3.6 | V |
| USB1.1 Transceiver（FS） | | | | | | |
| Input Levels（differential receiver） | | | | | | |
| V<sub>DI</sub> | Differential input sensitivity | ∣V<sub>I（DP）</sub>-V<sub>I（DM）</sub>∣ | 0.2 | | | V |
| V<sub>CM</sub> | Differential common mode voltage | | 0.8 | | 2.5 | V |
| Input Levels（single-ended receivers） | | | | | | |
| V<sub>SE</sub> | Single ended receiver threshold | | 0.8 | | 2.0 | V |
| Output levels | | | | | | |
| V<sub>OL</sub> | Low-level output voltage | | 0 | | 0.3 | V |
| V<sub>OH</sub> | High-level output voltage | | 2.8 | | 3.6 | V |

### Table 5.8 Dynamic characteristic：Analog I/O pins（DP/DM）

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Driver Characteristics | | | | | | |
| High-Speed Mode | | | | | | |
| $t_{HSR}$ | High-speed differential rise time | | 500 | | | ps |
| $t_{HSF}$ | High-speed differential fall time | | 500 | | | ps |
| Full-Speed Mode | | | | | | |
| $t_{FR}$ | Rise time | CL=50pF；10 to 90% of∣V<sub>OH</sub>-V<sub>OL</sub>∣； | 4 | | 20 | ns |
| $t_{FF}$ | Fall time | CL=50pF；90 to 10% of∣V<sub>OH</sub>-V<sub>OL</sub>∣； | 4 | | 20 | ns |
| $t_{FRMA}$ | Differential rise/fall time matching（$t_{FR}$ / $t_{FF}$） | Excluding the first transition from idle mode | 90 | | 110 | % |
| $V_{CRS}$ | Output signal crossover voltage | Excluding the first transition from idle mode | 1.3 | | 2.0 | V |

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## 5.6 Power Switch Feature

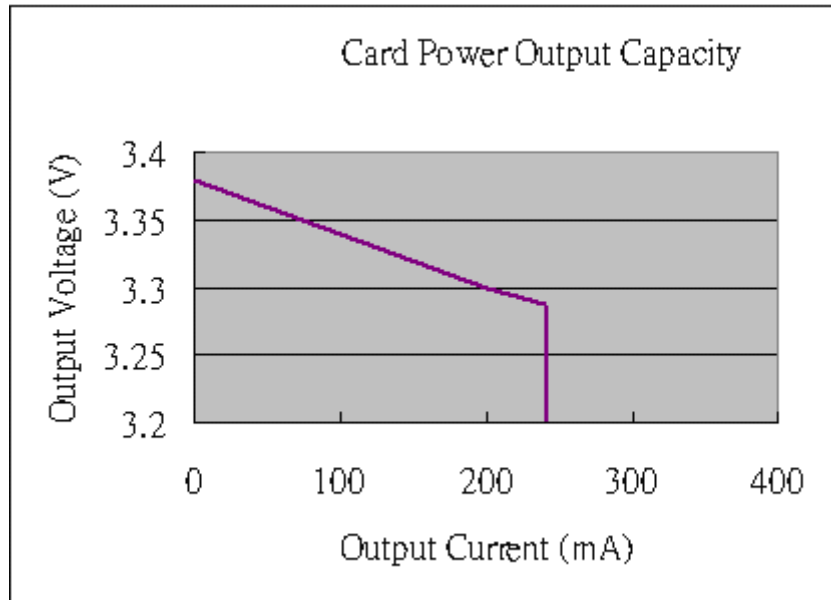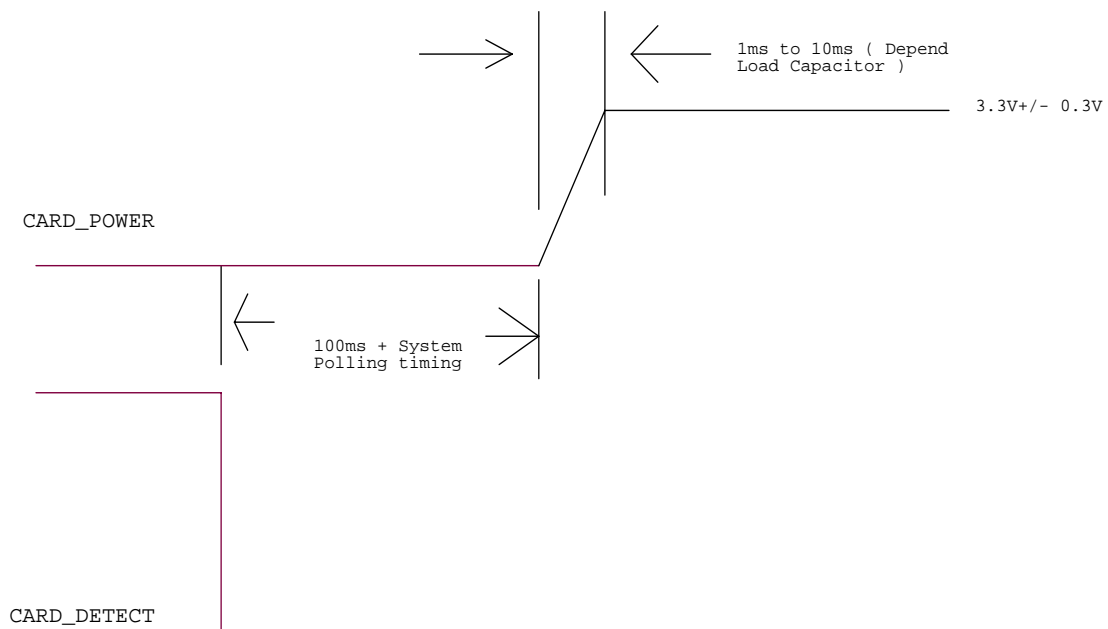**Figure 5.1 Card Power Switch Output Capacity**



**Figure 5.2 Card Detect Power-in Timing**

# 6. Mechanical Information

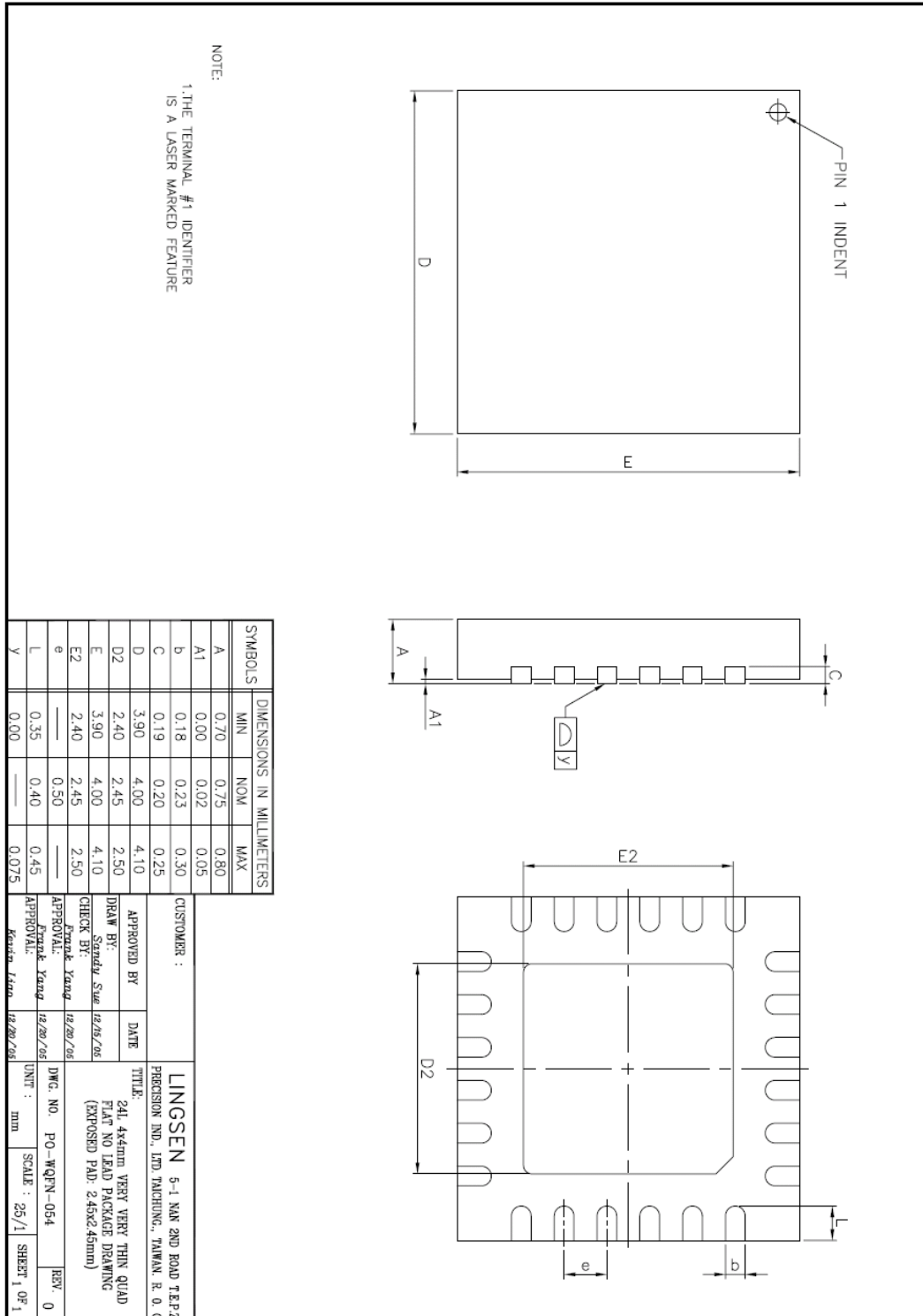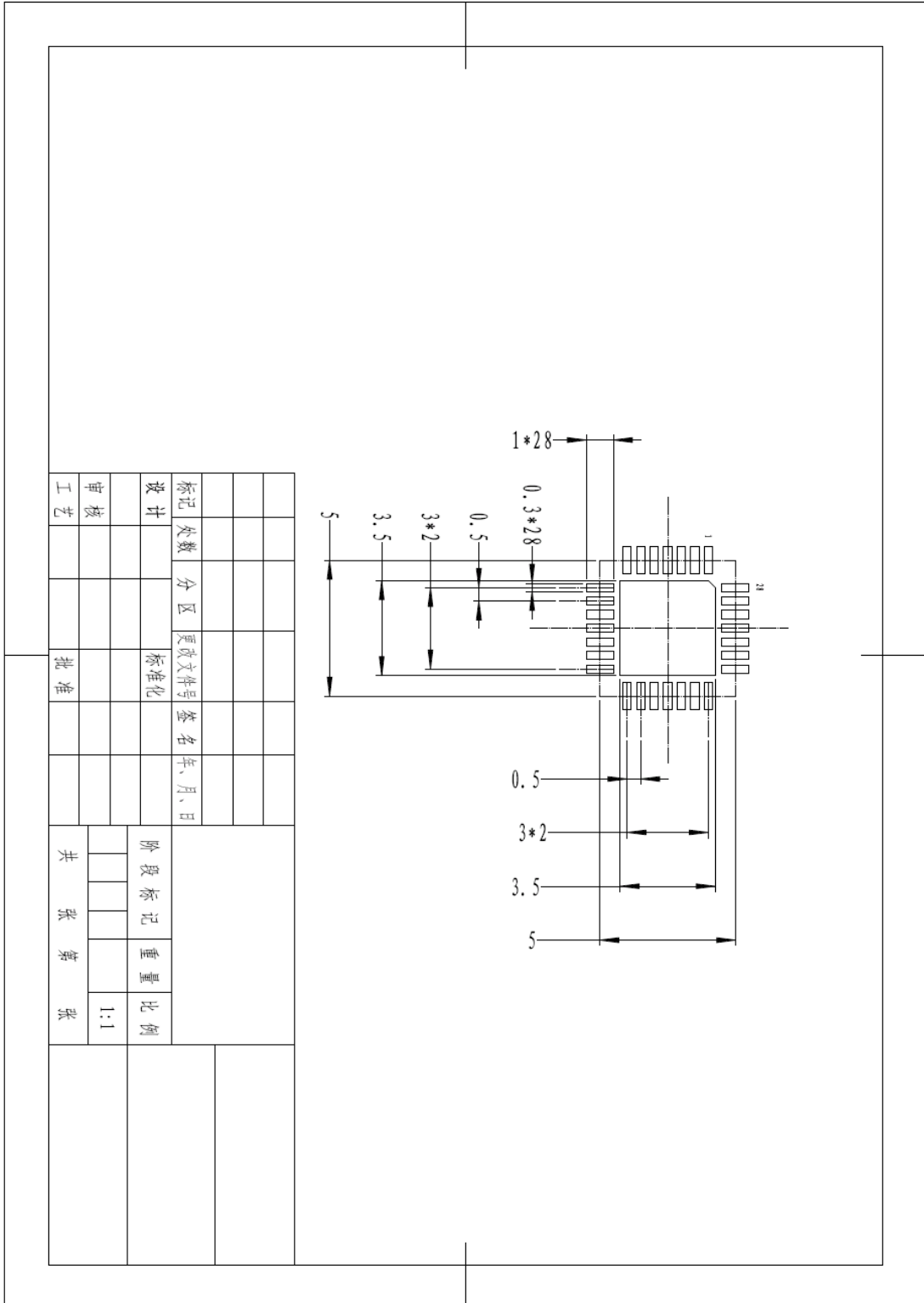**Figure 6.1 Mechanical Information Diagram**

**Figure 6.2 Layout Recommend**

# 7. Abbreviations

In this chapter some of the terms and abbreviations used throughout the technical reference manual are listed as follows.

**SIE**            Serial Interface Engine
**SD**             Secure Digital
**MMC**            Multimedia Card
**UTMI**           USB Transceiver Macrocell Interface

# About Alcor Micro, Corp.

Alcor Micro, Corp. designs, develops and markets highly integrated and advanced peripheral semiconductor, and software driver solutions for the personal computer and consumer electronics markets worldwide. We specialize in USB solutions and focus on emerging technology such as USB and IEEE 1394. The company offers a range of semiconductors including controllers for USB hub, integrated keyboard/USB hub and USB Flash memory card reader…etc. Alcor Micro, Corp. is based in Taipei, Taiwan, with sales offices in Taipei, Japan, Korea and California. Alcor Micro is distinguished by its ability to provide innovative solutions for spec-driven products. Innovations like single chip solutions for traditional multiple chip products and on-board voltage regulators enable the company to provide cost-efficiency solutions for the computer peripheral device OEM customers worldwide.